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PATENT APPLICATION

SCHOTTKY DIODE USING CHARGE BALANCE STRUCTURE

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CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of: (1) U.S. Application No. 10/666,034, filed September 18, 2003, entitled "Method for Forming a Semiconductor Structure with Improved Smaller Forward Voltage Loss and Higher Blocking Capability" which is a divisional application of U.S. Application No. 09/981,583, filed October 17, 2001, issued as U.S. Patent No. 6,677,641, and (2) U.S. Application No. 10/288,982, filed November 5, 2002, entitled "Trench Structure Having One or More Diodes Embedded Therein Adjacent a PN Junction and Method of Forming the Same", which disclosures are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates in general to semiconductor technology and in particular to Schottky diode structures and methods of manufacturing the same.

[0003] Schottky diodes are semiconductor devices which have a metal-semiconductor transition as their basic structure and whose basic electronic properties are defined by this transition. A Schottky diode is formed from a metal-semiconductor combination which is chosen such that a depletion zone arises at the boundary surface.

[0004] Fig. 1 shows a cross-section view of a portion of a conventional Schottky diode. Schottky diode **100** is formed by a metal layer **102** contacting a semiconductor region **104**. When Schottky diode **100** is turned on, current travels in a vertical direction from the metal layer **102** to the semiconductor region **104**. In such devices, the electric field decreases linearly from its maximum at the metal-semiconductor boundary surface, or Schottky barrier, through the semiconductor region **104** at a rate dictated by the doping concentration of the semiconductor region **104**. In addition, the semiconductor region **104** doping and thickness is tailored for a given blocking voltage, or breakdown voltage.

[0005] However, in the mid to high voltage range (e.g., 60 to 2000 volts), conventional Schottky diodes suffer from power loss primarily due to the high resistivity of the semiconductor region (e.g., semiconductor region **104** in Fig. 1). The semiconductor region has high resistivity because in order for the device to sustain the high voltages during the blocking state, the semiconductor region is lightly doped. The high resistivity of the

semiconductor region results in a higher on-resistance, which in turn results in high power loss. Since a high blocking voltage is a critical feature for mid to high voltage power devices, increasing the semiconductor region doping is not an option.

[0006] Thus, a technique which enables achieving a high device blocking capability, low on-resistance, and high current handling capability is desirable.

BRIEF SUMMARY OF THE INVENTION

[0007] In accordance with an embodiment of the invention, a Schottky diode includes a metal layer in contact with a semiconductor region to form a Schottky barrier therebetween. A first trench extends in the semiconductor region. The first trench includes at least one charge control electrode therein.

[0008] In another embodiment, the first trench further includes an insulating layer lining the trench sidewalls and bottom.

[0009] In another embodiment, the at least one charge control electrode is arranged in the first trench such that when the Schottky diode is biased in a blocking state, an electric field induced in the at least one charge control electrode influences an electric field in the semiconductor region to thereby increase the blocking voltage of the Schottky diode.

[0010] In accordance with another embodiment of the invention, a Schottky diode includes a metal layer in contact with a semiconductor region to form a Schottky barrier therebetween. A plurality of charge control electrodes is integrated with the semiconductor region so as to influence an electric field in the semiconductor region. At least two of the plurality of charge control electrodes is electrically decoupled from one another so as to be biased differently from one another.

[0011] In accordance with another embodiment of the invention, a Schottky diode includes a metal layer in contact with a semiconductor region to form a Schottky barrier therebetween. A first trench extends in the semiconductor region. The first trench includes at least one diode therein.

[0012] In one embodiment, the diode is reverse biased when the Schottky diode is in a blocking state.

[0013] In another embodiment, the first trench further includes an insulating layer which extends along sidewalls of the first trench but is discontinuous along the bottom of the first trench.

[0014] In another embodiment, the diode is arranged in the first trench such that when the Schottky diode is biased in a blocking state, an electric field induced in the at least one diode influences an electric field in the semiconductor region to thereby increase the blocking voltage of the Schottky diode.

[0015] In accordance with an embodiment of the present invention, a Schottky diode is formed as follows. A first trench extending in a semiconductor region is formed. At least one charge control electrode is formed in the trench. A metal layer is formed over the semiconductor region to form a Schottky barrier therebetween.

[0016] In accordance with an embodiment of the present invention, a Schottky diode is formed as follows. A first trench extending in a semiconductor region is formed. At least one diode is formed in the trench. A metal layer is formed over the semiconductor region to form a Schottky barrier therebetween.

[0017] These and other embodiments of the invention will be described with reference to the accompanying drawings and following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 shows a cross-section view of a conventional Schottky diode;

[0019] Fig. 2 shows a cross-section view of a Schottky diode structure having trenches with charge control electrodes therein in accordance with an embodiment of the present invention;

[0020] Figs. 3 shows a cross-section view of a Schottky diode having trenches with diodes therein in accordance with another embodiment of the present invention;

[0021] Figs. 4A and 4B respectively show a variation of the Schottky diode embodiments in Figs. 2 and 3;

[0022] Figs. 5 and 6 are graphs respectively showing the electric field through diode trenches and the semiconductor regions between adjacent trenches of an exemplary embodiment of the Fig. 3 Schottky diode structure;

[0023] Figs. 7A-7C show top views of three exemplary layout designs of the structures shown in Figs. 2 or 3;

[0024] Fig. 8A-8I show cross-section views at different processing stages of forming a Schottky diode structure having trenches with stacked charge control electrodes therein in accordance with an embodiment of the invention; and

[0025] Fig. 9A-9F show cross-section views at different processing stages of forming a Schottky diode structure having trenches with diodes therein in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Embodiments of the invention are directed to semiconductor devices and in particular to Schottky diode structures and methods of manufacturing the same.

[0027] Schottky diodes comprise a metal layer, such as Titanium, Platinum, Gold, Chromium, Palladium, Nickel, and a semiconductor region, such as Silicon, Gallium Arsenide, Silicon Carbide, or Gallium Nitride. The junction between the metal layer and the semiconductor region forms a Schottky barrier.

[0028] In embodiments of the invention, the Schottky diode includes one or more charge control electrodes. The charge control electrodes may be biased to control the electric field within the semiconductor region. In some embodiments, these charge control electrodes may be referred to as "field plates". The spacing and arrangement of the charge control electrodes can be set up in various stripe or cellular designs. In some embodiments, the sidewalls of each charge control electrode may be substantially parallel.

[0029] The charge control electrodes are stacked and buried within the semiconductor region. The stack of charge control electrodes is oriented generally vertically with respect to the major surface of the semiconductor region. A dielectric material insulates each of the charge control electrodes from the semiconductor region.

[0030] In some embodiments of the invention, there may be one or a more charge control electrodes. The charge control electrodes can be arranged in a plurality of groups with each group being embedded in a separate dielectric material structure. These different groups of charge control electrodes can be located at any suitable place in the semiconductor device. For example, the different pluralities of stacked charge control electrodes can be disposed at

the center of the semiconductor region, and/or to the side of the semiconductor region. The different pluralities of charge control electrodes can function independently of each other or together to alter the electric field within the semiconductor region.

[0031] In one embodiment, each charge control electrode in one group of charge control electrodes is adapted to be biased differently than the other charge control electrodes in the same group of charge control electrodes. The differently biased charge control electrodes can be used to adjust the electric field within the semiconductor region. When a Schottky diode, according to an embodiment of the invention, is in a blocking state, for example, the charge control electrodes within a group of charge control electrodes can be differently biased to maintain a substantially uniform and high electric field within the semiconductor region. By maintaining a substantially uniform electric field within the semiconductor region, the breakdown voltage of the semiconductor device is increased. Thus, for the same breakdown voltage, the semiconductor region can be highly doped to reduce the on-resistance. Accordingly, in embodiments of the invention, semiconductor devices having high breakdown voltages and/or low on-resistance properties can be produced.

[0032] In yet other embodiments, a Schottky diode structure has a trench with one or more diodes embedded therein (referred to hereinafter as "the diode trench structure"). Much like the charge control electrodes, the one or more embedded diodes advantageously influence the electric field within the semiconductor region to improve the breakdown voltage. The diode trench structure may be integrated in Schottky diode devices required to withstand high voltages. The diode trench structure helps achieve high breakdown voltages and/or low on-resistance properties.

[0033] Embodiments of the invention have a number of advantages over conventional Schottky diodes. In embodiments of the invention, the charge control electrodes or embedded diodes are used for charge spreading in the semiconductor region. For example, in the case of charge control electrodes, the bias of the charge control electrodes can be set precisely to control charge spreading in the semiconductor region of a device. Consequently, the maximum electric field in the semiconductor substrate can be much greater than about 2×10^5 V/cm, the maximum practical electric field achievable by superjunction devices. In some embodiments of the invention, the maximum electric field that can be created in the semiconductor region is limited by the ability of the dielectric material surrounding the charge control electrodes to support the voltages of the charge control electrodes. The

maximum electric field achievable in some embodiments of the invention can easily exceed 3.5×10^5 V/cm, a value greater than the electric field achievable in superjunction devices. Another advantage of the proposed structures is the relative ease of making narrow charge distribution regions in the semiconductor region. This improves the usage and efficiency of the semiconductor region. Furthermore, in embodiments of the invention, the Schottky diodes can have breakdown ratings in the low to mid voltage ranges, while exhibiting low on-resistance. For example, for a 150V Schottky diode, the on-resistance per unit area of some embodiments of the invention has been simulated to be 50% less than the on-resistance per unit area of conventional 150V Schottky diodes. While superjunction devices have low on-resistance properties, the precise doping requirements of superjunction devices have prevented them from being made with breakdown voltage ratings in lower to mid voltage ranges (e.g., < 200 V).

[0034] Using differently biased charge control electrodes or reverse biased trench diode structures in the semiconductor region of the Schottky diode substantially "flattens" out the electric field profile across the semiconductor region. If the charge control electrodes or trench diode structures are not present, the electric field profile would be "triangular" across the semiconductor region. In a conventional device, the electric field is at a maximum at the Schottky barrier junction and then decreases linearly from the Schottky barrier junction into the depth of the semiconductor region. By causing the electric field profile to be flatter (i.e:, more uniform) across the semiconductor region of a semiconductor device, a higher breakdown voltage is obtained. As will be shown, by using multiple charge control electrodes in each trench or multiple diodes in each trench, multiple spikes are induced in the electric filed profile along the depth of the semiconductor region. This increase in the electric field results in a larger area under the electric field curve, which in turn results in a higher breakdown voltage. In general, the use of more charge control electrodes or more diodes in each trench in the semiconductor region can result in a more uniform electric field in the semiconductor region.

[0035] Fig. 2 shows a cross-sectional view of a Schottky diode structure **200** having a plurality of trenches **210(a)-210(d)** in accordance with one embodiment of the invention. A semiconductor region **204** (e.g., an epitaxial layer) is formed over and is of the same conductivity type as a substrate **206**. A metal layer **202** overlies semiconductor region **204** to form a Schottky barrier therebetween. The plurality of trenches **210(a)-210(d)** extends from a top surface of semiconductor region **204** through to substrate **206**. Trenches **210(a)-210(d)**

may alternatively be terminated at a shallower depth or could extend deeper into substrate **206**.

[0036] A first plurality of charge control electrodes **212(a)-212(b)**, a second plurality of charge control electrodes **214(a)-214(b)**, a third plurality of charge control electrodes **216(a)-216(b)**, and a fourth plurality of charge control electrodes **218(a)-218(b)** are respectively disposed in first, second, third, and fourth trenches **210(a)-210(d)**. The charge control electrodes within a common trench are shown in a stacked relationship. The charge control electrodes are separated from each other and from the semiconductor region **204** by the dielectric material **208(a)-208(d)** within each of trenches **210(a)-210(d)**. Dielectric material **208(a)-208(d)** may comprise one or more of, for example, silicon dioxide, silicon nitride, and glass. Charge control electrodes within different pluralities of charge control electrodes can be at about the same vertical distance from the major surface **252**. For example, charge electrodes **212(a)**, **214(a)**, **216(a)**, and **218(a)** may be at the same vertical position within the semiconductor region **204**.

[0037] Although the exemplary embodiment shown in Fig. 2 shows four trenches **210(a)-210(d)**, it is understood that any suitable number of trenches, and typically a large number of trenches, are present in the Schottky diode structure. Each charge control electrode may be formed of any suitable material, such as doped or undoped polysilicon, or metal. Although two charge control electrodes are shown in each of the trenches **210(a)-210(d)** in the embodiment illustrated in Fig. 2, it is to be understood that any suitable number of charge control electrodes can be present in each trench. In general, a more uniform electric field can be obtained in semiconductor region **204** if there are more charge control electrodes per stack of charge control electrodes. This is described in more detail further below.

[0038] Each of charge control electrodes **212(a)-212(b)**, **214(a)-214(b)**, **216(a)-216(b)**, **218(a)-218(b)** can be individually biased with biasing elements (not shown) that may be formed in or on semiconductor substrate **206**. The biasing elements may bias the charge control electrodes **212(a)-212(b)**, **214(a)-214(b)**, **216(a)-216(b)**, **218(a)-218(b)** at potentials that are different from metal layer **202** and/or semiconductor substrate **206**. Any suitable biasing element could be used to bias the charge control electrodes. For example, the biasing elements can be resistors with different resistance values in a voltage divider. Alternatively, the biasing elements could be a series of diodes with different voltage ratings. Examples of suitable diodes can be found in U.S. Patent No. 5,079,608, which is herein incorporated by

reference in its entirety. In some embodiments, the biasing elements may be coupled to metal layer **202**. For example, metal layer **202** could be tapped with the biasing elements to provide charge control electrodes **212(a)-212(b), 214(a)-214(b), 216(a)-216(b), 218(a)-218(b)** with appropriate bias voltages. The biasing elements could also be coupled to the substrate **206.**

[0039] The biased charge control electrodes **212(a)-212(b), 214(a)-214(b), 216(a)-216(b), 218(a)-218(b)** in each trench **210(a)-210(b)** are used to advantageously alter the electrical field within the semiconductor region **204**. When the Schottky diode structure **200** is in the blocking state (i.e., reverse biased), the biased charge control electrodes **212(a)-212(b), 214(a)-214(b), 216(a)-216(b), 218(a)-218(b)** alter the electrical field within the semiconductor region **204** so that the resulting electrical field profile in semiconductor region **204** is higher and more uniform than if no charge control means were present in semiconductor region **204**. In one embodiment, biased charge control electrodes **212(a)-212(b), 214(a)-214(b), 216(a)-216(b), 218(a)-218(b)** alter the electrical field within semiconductor region **204** so that the electrical field is high and is substantially uniform throughout a substantial portion of semiconductor region **204** or at least in the zones where current flows through semiconductor region **204** from metal layer **202** to substrate **206.**

[0040] Further, by properly biasing the charge control electrodes and selecting proper thickness for dielectric material **208**, the charge spreading in semiconductor region **204** can be improved. In one embodiment, the charge control electrodes are connected to ground potential or to the anode potential and the dielectric thickness on each electrode is adjusted to achieve optimum charge balance in semiconductor region **204**. In an alternate embodiment, an optimum uniform thickness is selected for dielectric material 208, and the electrodes in each trench are biased to appropriate potentials to achieve charge balance. In yet another embodiment, both the thickness of the dielectric material on each electrode and the potential of each electrode are independently adjusted to achieve optimum charge balance.

[0041] Fig. 3 shows a cross-section view of a Schottky diode structure **300** having a plurality of trenches **310(a)-310(d)** in accordance with another embodiment of the present invention. A semiconductor region **304** (e.g., an epitaxial layer), is formed over and is of the same conductivity type as a substrate **306**. Semiconductor region **304** forms a Schottky barrier with metal layer **302**. A plurality of trenches **310(a)-310(d)** extends from a top surface of the semiconductor region **304** to substrate **306**. Trenches **310(a)-310(d)** may alternatively be terminated at a shallower depth or could extend deeper into substrate **306.**

[0042] Trenches **310(a)-310(d)** include diodes made up of opposite conductivity type regions **312** and **314** forming a pn junction **316** therebetween. Doped polysilicon or n-type and p-type silicon may be used to form regions **312** and **314**. Other material suitable for forming such trench diodes (e.g., Silicon Carbide, Gallium Arsenide, Silicon Germanium) may also be used. The trench diodes are insulated from semiconductor region **304** by insulating material **308(a)-308(h)** extending along the sidewalls of trenches **310(a)-310(d)**. Oxide may be used as insulating material **308(a)-308(h)**. As shown in Fig. 3, there is no insulating material along the bottom of trenches **310(a)-310(d)** thus allowing the bottom region **312** of the bottom trench diode to be in electrical contact with the underlying substrate **306**. The thickness of insulating material **308(a)-308(h)**, in one embodiment, is determined by such factors as the voltage that insulating material **308(a)-308(h)** is required to sustain and the extent to which the electric field in the trench diode is to be induced in semiconductor region **304(a)-304(e)** (i.e., the extent of coupling through the insulating layer).

[0043] Although four trenches **310(a)-310(d)** are shown in Fig. 3, it is to be understood that any suitable number of trenches can be, and typically many more trenches are, present in the semiconductor structure. Also, although three diodes are shown in each of trenches **310(a)-310(d)** in Fig. 3, it is to be understood that any suitable number of diodes can be present in each trench.

[0044] When Schottky diode **300** is reverse biased, the diodes embedded in trenches **310(a)-(d)** are reverse biased and thus the electric field is higher at the diode junctions **316** in the trenches. Through insulating layer **308(a)-(h)**, the electric field in the trench diodes induces a corresponding electric field in regions **304(a)-304(e)**. The induced field is manifested in regions **304(a)-304(e)** in the form of up-swing spikes and a general increase in the electric field curve in regions **304(a)-304(e)**. This results in an electric field curve which tapers down from its highest level at the major surface **352** at a far lower rate than in conventional structures. A trapezoidal-shaped area can thus be obtained under the electric field curve in regions **304(a)-304(e)** as opposed to the conventional triangular shape. A far greater breakdown voltage is thus obtained.

[0045] When Schottky diode structure **300** is biased in the conduction state, current passes through regions **304(a)-304(e)**. The electric filed across the reverse-biased trench diodes influence the charge distribution in regions **304(a)-304(e)** such that a more uniform charge spreading is obtained in regions **304(a)-304(e)**. That is, the amount of charge remains

relatively uniform across regions **304(a)-304(e)**. By spreading the charge more uniformly in regions **304(a)-304(e)**, the silicon area taken up by regions **304(a)-304(e)** is more efficiently used. Hence, for the same size regions **304(a)-304(e)**, the portion of the device on-resistance attributable to regions **304(a)-304(e)** is, in effect, reduced. This enables reducing the cell pitch for the same on-resistance. Generally, reverse biasing of the trench diodes can be achieved by connecting any of the N-type regions in the diode trenches to a high potential, or alternatively connecting any of the P-type regions in the trenches to a low potential.

[0046] Accordingly, trenches **310(a)-(d)** enable optimizing structure **300** to have higher breakdown voltage, lower on-resistance, and smaller cell pitch than can be achieved by conventional techniques.

[0047] Figs. 4A and 4B show a variation of the Schottky diode embodiments in Figs. 2 and 3, respectively. In Fig. 4A, lightly-doped shallow regions **205** are formed at an upper surface area of semiconductor region **204** between adjacent trenches **210**. Shallow regions **205** have the same conductivity type as but lower doping concentration than semiconductor region **204**. Shallow regions **205** may be formed using conventional techniques such as implanting sufficient counter-dopants at the surface area to reduce the doping concentration at the silicon to metal interface to less than that of semiconductor region **204**. In one embodiment, shallow regions **205** have a depth of in the range of 0.1-0.5μm.

[0048] Lightly-doped shallow regions **205** increase the barrier height at the Schottky junction thus advantageously minimizing the leakage current during the device blocking state. This in turn allows a higher doping concentration to be used in semiconductor region **204** thus reducing the diode on-resistance without degrading the blocking capability of the diode. Fig. 4B shows similarly integrated lightly-doped shallow regions **305** in the Schottky diode embodiment of Fig. 3.

[0049] Referring to Fig. 2, each of the charge control electrodes in each trench induces an electric filed increase in the corresponding area of adjacent semiconductor regions such that a substantially uniform electric field is obtained in the semiconductor regions between adjacent trenches. The net effect of the electric field increase caused by each charge control electrode is that the conventional triangular-shaped electric field in the semiconductor region is changed to a trapezoidal-shape. Thus, the area under the electric field curve is increased resulting in a higher breakdown voltage. With each charge control electrode causing a local increase in the electric field in corresponding adjacent semiconductor regions, the top of the

electric field waveform has a saw-tooth or saddled appearance. By using more charge control electrodes in each trench, the top of the electric field waveform could be made flatter and less saddled.

[0050] Illustratively, Figs. 5 and 6 show the electric field curve through diode trenches **310a,b,c,d** (Fig. 3) and through semiconductor regions **304a,b,c,d,e**, respectively. The vertical axis in Figs. 5 and 6 represents electric field and the horizontal axis represents dimension. In Fig. 5, the horizontal axis from left to right corresponds to the vertical dimension through the diode trench from top to bottom. In Fig. 6, the horizontal axis from left to right corresponds to the vertical dimension from the top surface **352** through the semiconductor regions **304a,b,c,d,e** to the substrate **306**.

[0051] As shown in the Fig. 5 graph, the reverse-bias across the trench diodes results in an electric field peak at each diode junction. Each of these electric field peaks induces a corresponding electric filed increase in a corresponding area of the adjacent semiconductor region as shown in the Fig. 6 graph. An almost trapezoidal-shaped area under the electric field curve is thus obtained, which is substantially greater than the area under the triangular-shaped electric field curve for conventional diode structures. Thus, a substantial increase in the breakdown voltage is achieved. The larger the number of diodes embedded in the trench, the greater would be the number of peaks in the electric filed in semiconductor regions **304a,b,c,d,e**, and thus the higher would be the area under the curve. The higher breakdown voltage enables the doping concentration of semiconductor region **304** (conventionally kept low to obtain the necessary breakdown voltage) to be increased to reduce the on-resistance.

[0052] The following table sets forth the values used for some of the simulation parameters. These values are merely exemplary and not intended to be limiting.

Parameter	Value
Epi doping	2×10^{15} cm^{-3}
Diode doping (N-type and P-type)	1×10^{16} cm^{-3}
Thickness of each of the N-type and P-type regions in diode trenches	0.5 μm
Thickness of oxide along trench sidewalls	500Å
Thickness of gate oxide	500Å

[0053] In embodiments with trench diodes or charge control electrodes, spacings and trench arrangement can be implemented in various stripe or cellular designs. A top view of three exemplary layout designs are shown in Figs. 7A, 7B, and 7C. In Fig. 7A, trenches **710(a)** are offset from one another, while Fig. 7B shows trenches **710(b)** to be aligned and arranged along rows and columns. In Fig. 7C, horizontally-extending trenches **710(c)** are arranged as parallel stripes. Diode or electrode regions **714(b)** insulated from one another by insulating material **716(b)** are laterally spaced from each other in each trench stripe **710(b)**. Although the trench regions and the diodes or electrodes embedded therein are shown as square or rectangular shaped regions, they may be designed as circular, oval, hexagonal, or any other geometric shape that is desired. Thus, many different designs, configurations, and geometric shapes can be envisioned by one skilled in the art in light of this disclosure.

[0054] Other embodiments of the invention are directed to methods for forming Schottky diodes with charge control electrodes and trench diodes. Exemplary method embodiments for forming stacked charge control electrodes within a trench in a semiconductor substrate are described next with reference to Figs. 8A to 8I.

[0055] In Fig. 8A, a trench **802** is etched in a semiconductor region **800** using conventional techniques such as an anisotropic etching process. A first oxide layer **804** is then formed to line the trench sidewalls and bottom and extend over the surface of semiconductor region **800**. The first oxide layer **802** can be formed by, for example, an oxidation process or deposition process such as chemical vapor deposition (CVD).

[0056] In Fig. 8B, a polysilicon layer **810** is formed to fill trench **802**. Next, as shown in Fig. 8C, polysilicon layer **810** is then recessed using conventional polysilicon etching techniques to form a first charge control electrode **808**. Polysilicon layer **810** may be etched using, for example, a dry RIE (reactive ion etch) process. The first charge control electrode **808** is disposed well below the major surface **830** of semiconductor region **800** and is buried within the semiconductor region **800**.

[0057] In Fig. 8D, a dielectric material **814** is deposited to fill trench **802**. Dielectric material **814** may comprise, for example, glass such as BPSG (borophosphsilicate glass) or BSG (borosilicate glass). If glass is used, the glass can be deposited using, for example, a vapor deposition process with a subsequent reflow step. In the reflow step, the entire structure is heated to flow the glass so that it can fill the empty spaces of trench **802**. Alternatively, silicon oxide or silicon nitride could be used as dielectric material **814**.

[0058] In Fig. 8E, dielectric material **814** is etched with a suitable etchant in another recess etch process such that a dielectric layer **816** remains on the first charge control electrode **808**. Dielectric layer **816** can serve as a barrier between the first charge control electrode **808** and a later formed second charge control electrode.

[0059] In Fig. 8F, a second oxide layer **818** is formed on the semiconductor region **800**. Similar to first oxide layer 804, the second oxide layer **818** can be formed using an oxidation process or a CVD. In Fig. 8G, another polysilicon layer **820** is formed to fill trench **802**. Polysilicon layer **820** can be formed in the same or different manner as the previously described polysilicon layer **810**.

[0060] In Fig. 8H, another recess etch process is performed to form a second charge control electrode **822**. The second charge control electrode **822** is disposed below the major surface **830** of semiconductor region **800**. Both the first and second charge control electrodes **808**, **822** are insulated from each other and from semiconductor region **800**.

[0061] In Fig. 8I, an insulating material fills the trench over the second charge control electrode **822**. It is apparent that the general process sequence described herein could be used to form additional charge control electrodes on top of the second charge control electrode **822** or along the sides of the first and second charge control electrodes. The remaining process steps for forming the top metal layer and the other structural features of the Schottky diode are carried out in accordance with conventional techniques and methods. In one embodiment, semiconductor region **800** is an epitaxial layer formed over a substrate (not shown). In the embodiment wherein lightly-doped shallow regions are to be formed at the Schottky interface as shown in Fig. 4A, a conventional counter-dopant implant is carried out after the step depicted by Fig. 8I but before forming the metal layer. The formation of the shallow regions is not limited to this particular stage, and may be carried out at an earlier or later stage of the process.

[0062] Other embodiments of the invention are directed to methods for forming Schottky diodes with trenches having diodes therein. Exemplary method embodiments for forming diodes within a trench in a semiconductor region are described with reference to Figs. 9A to 9F. In Fig. 9A, an epitaxial layer **904** is formed over substrate **906** using conventional methods. A trench mask defining a trench opening is then formed by depositing and patterning a photoresist layer (not shown). Silicon is removed from the defined trench opening to form trench **910**. The trench surfaces are then cleaned and a thin layer of thermal

oxide is grown inside the deep trench. A thicker (e.g. 200-600nm) insulating layer (e.g., CVD oxide) is then deposited over the thin layer of thermal oxide. The sidewalls of the trench are thus lined with an insulating layer **916**. The insulating material along the bottom of the trench is then removed. A suitable spacer material (e.g., nitride) may be used to protect the insulating material along the trench sidewalls during removal of insulation material at the trench bottom.

[0063] In the embodiment wherein doped polysilicon is used to form the trench diode, as in Figs. 9B-9E, the diode (made up of regions **912** and **914** of opposite conductivity type) is formed by performing a two step process of polysilicon deposition (Figs. 9B and 9D) followed by polysilicon etch (Figs. 9C and 9E). In the embodiment wherein the trench diode is from silicon material, the diode is formed by performing silicon deposition for each diode region using conventional selective epitaxial growth techniques. The steps for forming the diode can be repeated to form additional diodes in the trench. If a large number of stacked polysilicon diodes is required, a cluster tool commonly used to combine the steps of polysilicon deposition and polysilicon etch may be used to speed up the processing time.

[0064] In Fig. 9F, a metal layer **902** is then formed on epitaxial layer **904** using conventional techniques. In the embodiment wherein lightly-doped shallow regions are to be formed at the Schottky interface as shown in Fig. 4B, a conventional counter-dopant implant is carried out before forming the metal layer.

[0065] Regions **912** and **914** in trench **910** (Fig. 9F) may be n-type and p-type respectively, or alternatively their conductivity type may be reversed. Also, either of regions **912** and **914** may be independently biased if desired by, for example, extending one or both regions along the third dimension (i.e., perpendicular to the page) and then up to the silicon surface where contact can be made to them. Although only two regions of opposite conductivity is shown in trench **910**, three regions forming an npn or pnp stack, or any number of regions of alternating conductivity type may be formed in trench **910**. Further, as many trenches as needed may be formed. In one embodiment, substrate **906** and epitaxial layer **904** are of n-type conductivity, and epitaxial layer has a lower doping concentration than substrate **906**.

[0066] By properly designing the p-type and n-type regions of the trench diode, the trench diode's advantageous impact on charge spreading in the epitaxial layer **904** can be enhanced. Two factors impacting the charge spreading are the avalanche breakdown voltage of the trench diode and the width of the depletion region in the trench diode. For example, by

selecting proper doping concentration for each of the p-type and n-type regions of the trench diode, a high avalanche breakdown voltage can be obtained so that a maximum electric field of much greater magnitude than the conventional 2 x 10^5 V/cm can be obtained. The limitation in obtaining the maximum electric field then becomes the ability of insulating layer **916** to withstand high voltages. This limitation can however be eliminated by the proper design of insulating layer **916**. Typical gate oxide layers have a maximum electric field exceeding 3.5 x 10^5V/cm which suffices for many high voltage applications.

[0067] In alternate embodiments, trench **910** is made deeper to terminate at the interface between epitaxial layer **904** and substrate **906**, or alternatively, trench **910** is made yet deeper to extend clear through epitaxial layer **904** terminating within substrate **906**.

[0068] The cross-section views of the different embodiments may not be to scale, and as such are not intended to limit the possible variations in the layout design of the corresponding structures. Also, even though the Schottky diode embodiments herein are described in the context of vertically conducting structures, the principles of the present invention may be applied to laterally conducting Schottky diode structures. For example, the charge control electrodes could be integrated in lateral Schottky diode structures in a similar manner to those shown in the Figs. 5 and 6 structures of the above referenced U.S. Patent Number 6,777,641. Also, the trench structure with diodes therein could be integrated in lateral Schottky diode structures in a similar manner to that shown in the Fig. 7C structure of the above-referenced pending patent application No. 10/288,982, filed November 5, 2002, entitled "Trench Structure Having One or More Diodes Embedded Therein Adjacent a PN Junction and Method of Forming the Same."

[0069] Although a number of specific embodiments are shown and described above, embodiments of the invention are not limited thereto. For example, it is understood that the doping polarities of the structures shown and described could be reversed and/or the doping concentrations of the various elements could be altered without departing from the invention.

[0070] While the foregoing is directed to certain preferred embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope of the invention. Such alternative embodiments are intended to be included within the scope of the present invention. Moreover, the features of one or more embodiments of the invention may be combined with one or more features of other embodiments of the invention without departing from the scope of the invention.

[0071] Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claim, along with their full scope of equivalents.